

## MOS FIELD EFFECT TRANSISTOR NP80N04CHE, NP80N04DHE, NP80N04EHE

### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

### **DESCRIPTION**

These products are N-channel MOS Field Effect
Transistor designed for high current switching applications.

### **FEATURES**

- Channel temperature 175 degree rated
- Super low on-state resistance

 $R_{\text{DS(on)}} = 8.0~\text{m}\Omega~\text{MAX.}$  (Vgs = 10 V, Ip = 40 A)

- Low Ciss: Ciss = 2200 pF TYP.
- Built-in gate protection diode

### ORDERING INFORMATION

PART NUMBER	PACKAGE
NP80N04CHE	TO-220AB
NP80N04DHE	TO-262
NP80N04EHE	TO-263

### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage	VDSS	40	V
Gate to Source Voltage	Vgss	±20	V
Drain Current (DC) Note1	ID(DC)	±80	Α
Drain Current (Pulse) Note2	D(pulse)	±280	Α
Total Power Dissipation (T <sub>A</sub> = 25°C)	Рт	1.8	W
Total Power Dissipation (Tc = 25°C)	Рт	120	W
Single Avalanche Current Note3	las	52 / 31 / 13	Α
Single Avalanche Energy Note3	Eas	2.7 / 96 / 169	mJ
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C

- ★ Notes 1. Calculated constant current according to MAX. allowable channel temperature.
  - **2.** PW  $\leq$  10  $\mu$ s, Duty cycle  $\leq$  1 %
  - 3. Starting Tch = 25°C, Rg = 25  $\Omega$  , Vgs = 20 V  $\rightarrow$  0 V (See Figure 4.)

### (TO-220AB)



(TO-262)



(TO-263)



### THERMAL RESISTANCE

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

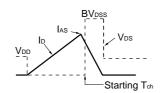


### **ELECTRICAL CHARACTERISTICS (TA = 25°C)**

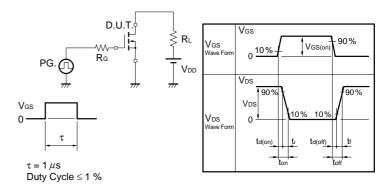
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CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)	Vgs = 10 V, ID = 40 A		6.2	8.0	mΩ
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	3.0	4.0	V
Forward Transfer Admittance	<b>y</b> fs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 40 A	15	31		S
Drain Leakage Current	Ipss	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			10	μΑ
Gate to Source Leakage Current	lgss	Vgs = ±20 V, Vps = 0 V			±10	μΑ
Input Capacitance	Ciss	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz		2200	3300	pF
Output Capacitance	Coss			490	730	pF
Reverse Transfer Capacitance	Crss			230	410	pF
Turn-on Delay Time	td(on)	$I_D = 40 \text{ A}, V_{GS(on)} = 10 \text{ V}, V_{DD} = 20 \text{ V},$		24	52	ns
Rise Time	<b>t</b> r	$R_G = 1 \Omega$		14	36	ns
Turn-off Delay Time	td(off)			44	88	ns
Fall Time	<b>t</b> f			15	37	ns
Total Gate Charge	Q <sub>G</sub>	ID = 80 A, VDD = 32 V, VGS = 10 V		40	60	nC
Gate to Source Charge	Qgs			12		nC
Gate to Drain Charge	Q <sub>GD</sub>		_	16		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	IF = 80 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 80 A, Vgs = 0 V, di/dt = 100 A/ $\mu$ s		40		ns
Reverse Recovery Charge	Qrr			50		nC

### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

# $\begin{array}{c} \text{D.U.T.} \\ \text{RG} = 25 \, \Omega \\ \text{PG.} \\ \text{Ves} = 20 \, \rightarrow 0 \, \text{V} \end{array} \right\} \stackrel{\text{D.U.T.}}{\geqslant} 50 \, \Omega$



### **TEST CIRCUIT 2 SWITCHING TIME**



### **TEST CIRCUIT 3 GATE CHARGE**

### TYPICAL CHARACTERISTICS (TA = 25°C)

Figure 1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

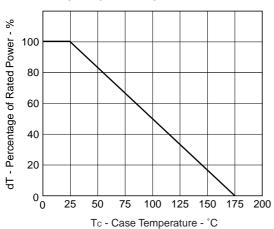
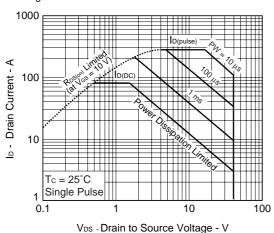


Figure.3 FORWARD BIAS SAFE OPERATING AREA



CASE TEMPERATURE

Figure 2. TOTAL POWER DISSIPATION vs.

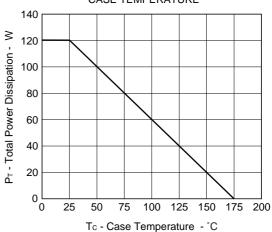


Figure 4. SINGLE AVALANCHE ENERGY **DERATING FACTOR** 

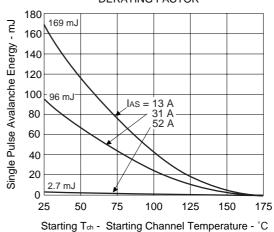


Figure 5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

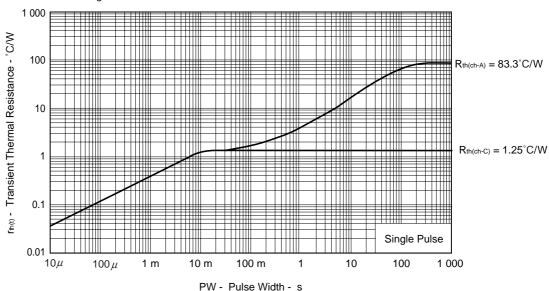


Figure 6. FORWARD TRANSFER CHARACTERISTICS

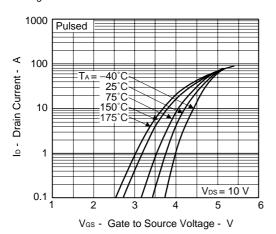


Figure 8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

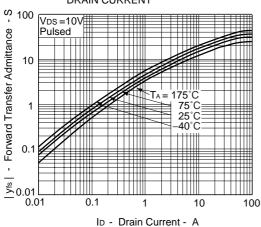


Figure 10. DRAIN TO SOURCE ON-STATE  $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$  - Drain to Source On-state Resistance -  $\mathsf{m}\Omega$ RESISTANCE vs. DRAIN CURRENT 20 Pulsed  $V_{GS} = 10 V$ 100 1000 ID - Drain Current - A

Figure 7. DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

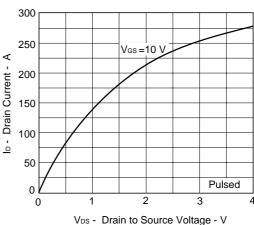


Figure 9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

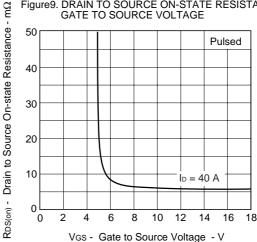
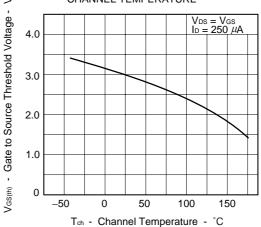
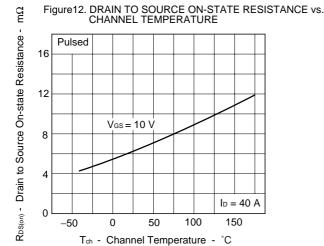
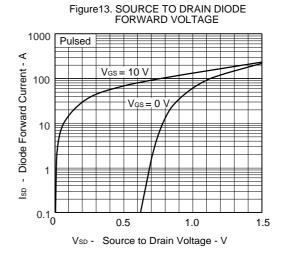
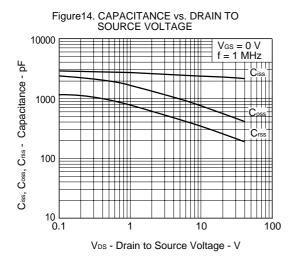


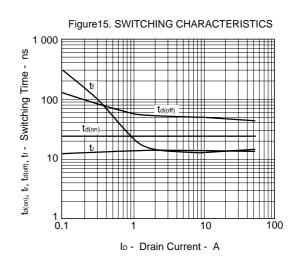
Figure11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

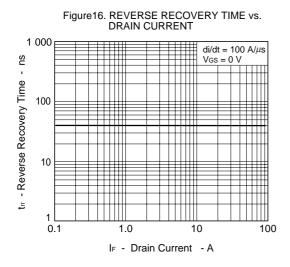


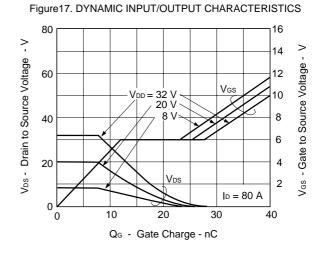






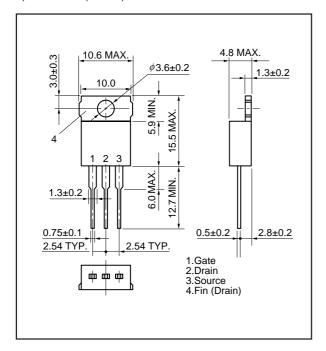




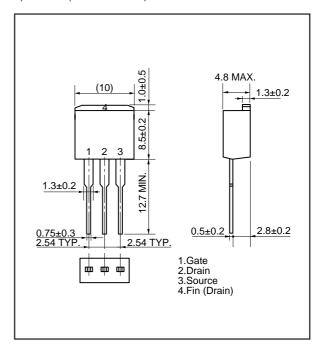


### PACKAGE DRAWINGS (Unit: mm)

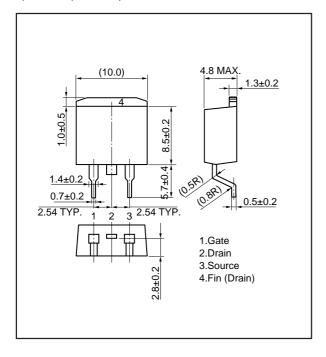
### 1) TO-220AB (MP-25)



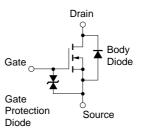
### 2) TO-262 (MP-25 Fin Cut)



### 3) TO-263 (MP-25ZJ)



### **EQUIVALENT CIRCUIT**



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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